Summary of the Invention

The present invention relates to an apparatus for changing a horizontal/vertical scanning frequency in a decoding block for restoring an MPEG signal. In an exemplary embodiment of the invention shown in Fig. 2, when I-picture data is received, the I-picture data is reverse quantized and reverse discrete cosine transformed in elements 201 and 202, respectively. The I-picture data is stored in the prediction memory 205 without being changed by adder 203. A P-picture is reversed discrete cosine transformed and input to the mixer 203 so that the error data of the P-picture is added to the data of the I-picture by the mixer 203 to obtain a forward prediction P-picture. The data of the forward predicted P-picture is stored in the second prediction memory 206 via the first switch 204. Then, the error data for bidirectionally predicting the B1-picture is input to the adder 203, and the I-picture stored in the first prediction memory 205 and the P-picture stored in the second 206 are read and mean calculated by the mean operator 208. The mean operator data is output to the mixer 203 through the second switching unit 209, and the error data for the bi-directional prediction is added to the bi-directional mean calculated data. The bidirectionally predicted B1-picture is output from the mixer 203 and stored in the B-picture memory 207 via the first switching unit 204. When the B1-picture data is stored in the B-picture memory 207, the frequency of the read clock signal of the first and second prediction memories 205 and 206 and the B-picture memory 207 is set to be double that of the general scanning method. Thus, the motion information transmitted from the transmitting side can be read twice as fast as in a general scanning method and the output can be twice as fast as the general scanning method.

In one embodiment of the invention shown in Fig. 4B, the field frequency can be double that of the general scanning method. Thus, it is possible to obtain a double scan converted output signal in which the vertical scanning frequency of the video signal is doubled.

In another embodiment of the invention, a progressive scan converting operation for producing a horizontal scanning frequency which is twice that of the general scanning frequency method may also be achieved.

Summary of Song et al

Song et al relates to a B-frame processing apparatus including a motion compensation apparatus in units of a half pixel. According to one embodiment of Song et al, shown in Fig. 1, when an I-frame is input, the I-frame data are inverse-quantized and IDCT-transformed by the restoring section 2 and then the restored data are stored in the first and third memories 12 and 14. After this, when the first P-frame P1 enters, the P-frame data is added by the adder 23 to the value which is motion compensated by the first frame memory 12, and stored in the second and fourth frame memories 13 and 25. When the first B-frame B1 enters, the value which is motion-compensated, respectively, by the first and second frame memories 12 and 13, is added by the adder 23 to the image signal inverse-quantized and IDCT-transformed. The added value is directly provided to the image processing section 28 through the slice buffer 27 without being stored in the frame memory. The next B-frame B2 is also provided to the image processing section 28 in the same way.

On the other hand, when the second P-frame P2 enters, the value which is motion-compensated by the second frame memory 13 is added by the adder 23 to the restored image data

which has been inverse-quantized and IDCT-transformed, and then the added value is stored in the first and third frame memories 12 and 14. At the same time, the data of the first P-frame P1 stored in the fourth memory 25 are read out and provided to the image processing section 28, thereby changing the display order of the image.

In another embodiment shown in Fig. 5, when the I-frame enters, the image signal of the I-frame is stored in the first frame memory 45 through the adder 56 and the bi-directional latch 52. The write address of the first frame memory 45 is generated by the write address generator 49. At this time, a data bus passes through the bi-directional latches 52 and 53, alternately with each frame and is stored in the respective frame memories, and the write address of the frame memory 46 corresponds to the address of the write address generator 49. When the P1-frame enters, the I-frame image signal which has been previously stored is read out from the first frame memory 45 and enters the adder 56 through the bi-directional latch 52 and is added to the P1-frame image signal. The added video signal passes through the bi-directional latch 53 again and is stored in the second frame memory 46. The read address of the first memory 45 may be generated by the first read address generator 50 utilizing motion vectors. The FIFO memory 57 can stored the P1-frame image signal and provide an I-frame image signal at the same time. Thereafter, when the B1-frame enters, the frame memories 45 and 46 stop the write operation and perform only image data read operation in accordance with read addresses provided from the read address generators 50 and 51. The image data having been read in accordance with read addresses from the read address generators 50 and 51 whose input are motion vectors, are provided through the bi-directionally buffers 52 and 53 and the provided image data are averaged

by the mean value calculating section 54. Multiplexor 55 provides the average image data, selectively to adder 56.

Analysis of the Claim Rejections

In rejecting claim 1 as being anticipated by Song et al, the Examiner cites element 52 of Fig. 5 of Song et al as disclosing a B-picture memory for storing B-picture data, the B-picture data having been bidirectionally prediction restored by the decoding block.

Applicant submits, however, that element 52 of Fig. 5 is not a memory for storing B-picture data. In more detail, element 52 is a bi-directional latch for storing the image signal of the I-frame in the first memory 45 (col. 10, lines 3-5), and for outputting the image data of the stored I-frame from frame memory 45 when a B-frame is processed (col. 10, lines 37-49). Applicant has not identified any disclosure in Song et al that bi-directional buffer 52 is used to store a B-picture.

In general, the operation of the claimed invention is significantly different from the operation of Song et al, at least in that the claimed invention stores B-picture data and reads out the B-picture data at an increased frequency so that the number of fields or lines displayed may be increased. On the other hand, Song et al stores I- and P-frame data and when B-frame data is introduced to the device, manipulates the stored I- and P-frame data and the received B-frame data to perform motion compensation in units of a half pixel.

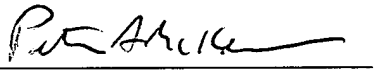
Applicant submits that claims 1-2 are not anticipated by Song et al, at least because this reference fails to teach the claimed B picture memory.

Applicant submits that claim 3 is not unpatentable over Song et al and Richards et al, at least because these references fail to teach or suggest the claimed B picture memory.

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,



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